## Chapter 4

## Introduction to Bipolar Junction Transistors (BJTs)

### 4.1 Introduction [5]

The transistor was invented by a team of three men at Bell Laboratories in 1947. Although this first transistor was not a bipolar junction device, it was the beginning of a technological revolution that is still continuing. All of the complex electronic devices and systems today are an outgrowth of early developments in semiconductor transistors. Two basic types of transistors are the bipolar junction transistor (BJT) and the field-effect transistor (FET). The BJT is used in two broad areas- as a linear amplifier to amplify an electrical signal and as an electronic switch.

### 4.2 Transistor Structure [5]

The BJT (bipolar junction transistor) is constructed with three doped semiconductor regions separated by two p-n junctions, as shown in the epitaxial planar structure in Figure 4.1(a). The three regions are called emitter (E), base (B), and collector (C).

Physical representations of the two types of BJTs are shown in Figure 4.1(b) and 4.1(c). One type consists of two $n$ regions separated by a p region (npn), and the other type consists of two p regions separated by n region ( pnp ). The term bipolar refers to the use of both holes and electrons as current carriers in the transistor structure.


Figure 4.1 Basic BJT construction. [5]

The pn junction joining the base region and the emitter region is called the base-emitter junction. The pn junction joining the base region and the collector region is called the base-collector junction, as indicated in Figure 4.1(b). A wire lead connects to each of the three regions, as shown. These leads are labeled E, B, and C for emitter, base, and collector, respectively. The base region is lightly doped and very thin compared to the heavily doped emitter and the moderately doped collector regions. Figure 4.2 shows the schematic symbols for the npn and pnp bipolar junction transistors.

(a) $n p n$

(b) $p n p$

Figure 4.2 Standard BJT (bipolar junction transistor) symbols. [5]

### 4.3 Basic Transistor Operation [5]

Figure 4.3 shows the proper bias arrangement for both npn and pnp transistors for active operation as amplifier. Notice that in both cases, the baseemitter (BE) junction is forwarded-biased and the base-collector (BC) junction is reverse-biased.


Figure 4.3 Forward-reverse bias of a BJT. [5]

## Transistor Currents

The directions and schematic symbol of the currents in an npn transistor and those for a pnp transistor are shown in figure 4.4. Notice that the arrow on the emitter of the transistor symbols points is the direction of convention current. These diagrams show that the emitter current $\left(\mathrm{I}_{\mathrm{E}}\right)$ is the sum of the collector current ( $\mathrm{I}_{\mathrm{C}}$ ) and the base current $\left(\mathrm{I}_{\mathrm{B}}\right)$, expressed as $\mathrm{I}_{\mathrm{E}}=\mathrm{I}_{\mathrm{C}}+\mathrm{I}_{\mathrm{B}}$


### 4.4 Transistor Characteristics and Parameters [5]

When the transistor is connected to dc bias voltage, as shown in Figure 4.5(a) for npn and Figure 4.5(b) for pnp types, $\mathrm{V}_{\mathrm{BB}}$ forward-biases the base-emitter junction, and $\mathrm{V}_{\mathrm{CC}}$ reverse-biases the base-collector junction.

(a) $n p n$

(b) $p n p$

Figure 4.5 Transistor DC bias circuit [5]

### 4.4.1 DC Beta ( $\beta_{\mathrm{DC}}$ ) and DC Alpha ( $\alpha_{\mathrm{DC}}$ )

The ratio of the dc collector current $\left(\mathrm{I}_{\mathrm{C}}\right)$ to the dc base current $\left(\mathrm{I}_{\mathrm{B}}\right)$ is the dc beta $\left(\beta_{\mathrm{DC}}\right)$ which is the dc current gain of a transistor.

$$
\beta_{D C}=\frac{I_{C}}{I_{B}}
$$

$\beta_{\mathrm{DC}}$ is usually designated as an equivalent hybrid (h) parameter, $\mathrm{h}_{\mathrm{FE}}$, on transistor data sheets. Therefore,

$$
h_{F E}=\beta_{D C}
$$

The ratio of the dc collector $\left(\mathrm{I}_{\mathrm{C}}\right)$ to the dc emitter current $\left(\mathrm{I}_{\mathrm{E}}\right)$ is the dc alpha ( $\alpha_{\mathrm{DC}}$ ). The alpha is a less-used parameter than beta in transistor circuits

$$
\alpha_{D C}=\frac{I_{C}}{I_{E}} \quad \text { or } \quad \alpha_{D C}=\frac{\beta_{D C}}{\beta_{D C}+1}
$$

Example 1: Determine the dc current gain $\beta_{\mathrm{DC}}$ and the emitter current $\mathrm{I}_{\mathrm{E}}$ for a transistor where $\mathrm{I}_{\mathrm{B}}=50 \mu \mathrm{~A}$ and $\mathrm{I}_{\mathrm{C}}=3.65 \mathrm{~mA}$.

## Solution:

$$
\begin{aligned}
& \beta_{D C}=\frac{I_{C}}{I_{B}}=\frac{3.65^{*} 10^{-3}}{50^{*} 10^{-6}}=73 \\
& \begin{array}{r}
I_{E}=I_{C}+I_{B}=3.65 \mathrm{~mA}+50 \mu \mathrm{~A} \\
\quad=3.70 \mathrm{~mA}
\end{array} \\
& \begin{array}{r}
\alpha_{D C}=\frac{\beta_{D C}}{\beta_{D C}+1}=\frac{73}{73+1}=0.9865
\end{array} \\
& \text { Or } \alpha_{D C}=\frac{I_{C}}{I_{E}}=\frac{3.65 \mathrm{~mA}}{3.70 \mathrm{~mA}}=0.9865
\end{aligned}
$$

### 4.4.2 Current and Voltage Analysis

Consider the basic transistor bias circuit configuration shown in Figure 4.6. Three transistor dc currents and three dc voltages can be identified.

- $\mathrm{I}_{\mathrm{B}}$ : dc base current
- $\mathrm{I}_{\mathrm{E}}$ : dc emitter current
- $\mathrm{I}_{\mathrm{C}}$ : dc collector current
- $\mathrm{V}_{\mathrm{BE}}$ : dc voltage at base with respect to emitter
- $\mathrm{V}_{\mathrm{CB}}$ : dc voltage at collector with respect to base
- $\mathrm{V}_{\mathrm{CE}}:$ dc voltage at collector with respect to emitter
$\mathrm{V}_{\mathrm{BB}}$ forward-biases the base-emitter junction and $\mathrm{V}_{\mathrm{CC}}$ reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of $\mathrm{V}_{\mathrm{BE}} \cong 0.7 \mathrm{~V}$. Since the emitter is at ground ( 0 V ), by Kirchhoff's voltage law, the voltage across $R_{B}$ is

$$
V_{R_{B}}=V_{B B}-V_{B E}
$$



Figure 4.6 Transistor currents and voltages. [5]

Also, by Ohm's law,

$$
V_{R_{B}}=I_{B} R_{B}
$$

Substituting for $V_{R B}$ yields

$$
I_{B} R_{B}=V_{B B}-V_{B E}
$$

Solving for $I_{B}$,

$$
I_{B}=\frac{V_{B B}-V_{B E}}{R_{B}}
$$

The voltage $V_{C E}$ is

$$
V_{C E}=V_{C C}-V_{R_{C}}
$$

Since the drop across $R_{C}$ is

$$
V_{R_{C}}=I_{C} R_{C}
$$

the voltage at the collector with respect to the emitter can be written as

$$
V_{C E}=V_{C C}-I_{C} R_{C}
$$

where $I_{C}=\beta_{D C} I_{B}$
The voltage across the reverse-biased collector-base junction is

$$
V_{C B}=V_{C E}-V_{B E}
$$

Example 2: Determine $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}, \mathrm{I}_{\mathrm{E}}, \mathrm{V}_{\mathrm{BE}}, \mathrm{V}_{\mathrm{CE}}$, and $\mathrm{V}_{\mathrm{CB}}$ in the circuit. Assume $\beta_{\mathrm{DC}}=$ 150.


Figure 4.7 For Example 2 [5]

## Solution:

$$
\begin{aligned}
& V_{B E}=0.7 \mathrm{~V} \quad(\text { forwardbias forn } \mathrm{p}-\mathrm{n}) \\
& I_{B}=\frac{V_{B B}-V_{B E}}{R_{B}}=\frac{5-0.7}{10 \mathrm{k} \Omega}=430 \mu \mathrm{~A} \\
& I_{C}=\beta_{D C} I_{B}=150^{*} 430 \mu \mathrm{~A}=64.5 \mathrm{~mA}
\end{aligned}
$$

$$
\left.\begin{array}{l}
I_{E}=I_{C}+I_{B}=64.5 \mathrm{~mA}+430 \mu \mathrm{~A}=64.9 \mathrm{~mA} \\
V_{C B}=V_{C C}-I_{C} R_{C}=10-(64.5 \mathrm{~mA} * 100 \Omega)=3.55 \mathrm{~V} \\
V_{C B}=V_{C B}-V_{B E}=3.55 \mathrm{~V}-0.7 \mathrm{~V}=2.85 \mathrm{~V} \\
V_{B E}=0.7 \mathrm{~V}, \text { forward bias } \\
V_{C B}=V_{C}-V_{B}=2.85 \mathrm{~V}, \text { reverse bias }
\end{array}\right\} \text { Mode active }
$$

Example 3: Determine $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}, \mathrm{I}_{\mathrm{E}}, \mathrm{V}_{\mathrm{BE}}, \mathrm{V}_{\mathrm{CE}}$, and $\mathrm{V}_{\mathrm{CB}}$ in the circuit. Assume $\beta_{\mathrm{DC}}=$ 150.


Figure 4.8 For Example 3

Solution:
Here ; $\mathrm{V}_{\mathrm{BE}}=0.7 \mathrm{~V}$
leflloop; $V_{B B}=V_{R B}+V_{B E}+V_{R E}=I_{B}(10 K \Omega)+0.7+I_{E}(5 K \Omega)$
$I_{E}=I_{C}+I_{B}=150 I_{B}+I_{B}=151 I_{B}$
$5=(10 K \Omega) I_{B}+0.7+(755 K \Omega) I_{B}$

$$
\begin{aligned}
& I_{B}=\frac{5-0.7 \mathrm{~V}}{(765 \mathrm{~K} \Omega)}=5.62 \mu \mathrm{~A} \\
& \begin{aligned}
I_{C} & =150 I_{B}=0.843 \mathrm{~mA} \\
I_{E} & =I_{C}+I_{B}
\end{aligned}=5.62 \mu \mathrm{~A}+0.843 \mathrm{~mA} \\
& \\
& \quad=0.8486 \mathrm{~mA}
\end{aligned}
$$

right loop ; $\mathrm{V}_{\mathrm{CC}}=I_{C} R_{C}+V_{C E}+I_{E} R_{E}$

$$
10=(0.843 \mathrm{~mA})(100 \Omega)+V_{C E}+(0.8486 \mathrm{~mA})(5 \mathrm{~K} \Omega)
$$

$$
10=0.843 \mathrm{~mA}+V_{C E}+4.243
$$

$$
V_{C E}=10-0.0843-4.243=5.6727 \mathrm{~V}
$$

$\qquad$ \#

$$
V_{C B}=V_{C E}-V_{B E}=5.6727-0.7=4.9727 \mathrm{~V}
$$

$\qquad$
$* V_{B E}=0.7 V$ forward bias
$V_{C B}=V_{C}-V_{B}=4.9727 \mathrm{~V}$, reverse bias

Example 4: Determine $\mathrm{I}_{\mathrm{E}}, \mathrm{V}_{\mathrm{BE}}, \mathrm{V}_{\mathrm{CE}}$, and $\mathrm{V}_{\mathrm{CB}}$ in the circuit. Assume $\beta_{\mathrm{DC}}=150$.


Figure 4.9 For Example 4

## Solution:

$$
\begin{aligned}
& V_{B E}=-V_{E B}=-0.7 V \ldots \\
& \text { mesh1; } V_{E B}+I_{B} R_{B}-V_{B B}=0 \Rightarrow I_{B}=\frac{V_{B B}-V_{E B}}{R_{B}} \\
& \quad I_{B}=\frac{3-0.7}{27 K} \approx 0.0852 \mathrm{~mA} \\
& \quad I_{C}=\beta_{D C} I_{B}=125^{*} 0.0852=10.65 \mathrm{~mA} \\
& \text { mesh2; } V_{E C}+I_{C} R_{C}-V_{C C}=0 \\
& \quad V_{E C}=V_{C C}-I_{C} R_{C}=8-10.65^{*} 10^{-3 * 390} \\
& \quad=3.8465 \mathrm{~V} \\
& V_{C E}=-V_{E C}=-3.8465 \mathrm{~V} \\
& \begin{aligned}
& V_{C B}= V_{C E}-V_{B E}=-3.8465-(-0.7) \\
&=-3.1465 \mathrm{~V} \\
& I_{E}=I_{C}+I_{B}=10.65 \mathrm{~mA}+0.0852 \mathrm{~mA} \\
&=10.7352 \mathrm{~mA}
\end{aligned}
\end{aligned}
$$

Practice Problem 1: Determine $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{E}}, \mathrm{I}_{10 k \Omega}, \mathrm{~V}_{\mathrm{B}}, \mathrm{V}_{\mathrm{C}}$, and $\mathrm{V}_{\mathrm{E}}$ in the circuit. Assume $\beta_{\mathrm{DC}}=100$.


Figure 4.10 For Practice problem 1

### 4.4.3 Modes of BJT Operation

A single PN junction has two different types of bias, forward bias and reverse bias. Therefore, a two-PN-junction device has four types of bias, as shown in Figure 4.11.


| CB Junction | BE Junction | Mode of Operation |
| :---: | :---: | :---: |
| Reverse | Reverse | Cut-off |
| Forward | Reverse | Inverted |
| Reverse | Forward | Active |
| Forward | Forward | Saturation |

Figure 4.11 four modes of BJT operation

### 4.4.4 Collector Characteristics Curves

Using a circuit like that shown in Figure 4.12, we can generate a set of collector characteristic curves that explain how $\mathrm{I}_{\mathrm{C}}$ varies with $\mathrm{V}_{\mathrm{CE}}$, for specified values of $\mathrm{I}_{\mathrm{B}}$. Notice in the circuit diagram that both $\mathrm{V}_{\mathrm{BB}}$ and $\mathrm{V}_{\mathrm{CC}}$ are variable source of voltage.


Figure 4.12 BJT circuit with variable voltage sources. [5]


Figure 4.13 Collector characteristic curves.

From Figure 4.13, assume that $V_{B B}$ is set to produce a certain value of $I_{B}$ and $\mathrm{V}_{\mathrm{CC}}$ is zero. For this condition, both the base-emitter junction and the basecollector junction are forward-biased because the base is at approximately 0.7 V (for Si ) while the emitter and the collector are at 0 V . Here, the base current is through the base-emitter junction because the low impedance path to ground, and $\mathrm{I}_{\mathrm{C}}$ is zero. When both junctions are forward-biased, the transistor is in the saturation region of its operation.

As $\mathrm{V}_{\mathrm{CC}}$ is increased, $\mathrm{V}_{\mathrm{CE}}$ increases gradually as the collector current increases. When $\mathrm{V}_{\mathrm{CE}}$ exceeds $\mathrm{V}_{\mathrm{K}}(0.7 \mathrm{~V}$ for Si$)$, the base-collector junction becomes reverse-biased and the transistor goes into the active or linear region of its operation. Once the base-collector junction is reverse-biased, $\mathrm{I}_{\mathrm{C}}$ remains essentially constant for a given value of $\mathrm{I}_{\mathrm{B}}$ as $\mathrm{V}_{\mathrm{CE}}$ continues to increase. For this region of the characteristic curve, the value of $\mathrm{I}_{\mathrm{C}}$ is determined only by the relationship expressed as $\mathrm{I}_{\mathrm{C}}=\beta_{\mathrm{DC}} \mathrm{I}_{\mathrm{B}}$.

When $\mathrm{V}_{\mathrm{CE}}$ reaches a sufficiency high voltage, the reverse-biased basecollector junction goes into breakdown; and the collector current increases rapidly. A transistor should never be operated in this breakdown region.

A family of collector characteristics curves is produced when $I_{C}$ versus $V_{C E}$ is plotted for several values of $I_{B}$, as shown in Figure 4.14. When $I_{B}=0$, the transistor is in the cutoff region although there is a very small collector leakage current.


Figure 4.14 A family of collector characteristics curves.

Example 5: Sketch an ideal family of collector curves for the circuit in Figure 4.15 for $\mathrm{I}_{\mathrm{B}}=5 \mu \mathrm{~A}$ to $25 \mu \mathrm{~A}$ in $5 \mu \mathrm{~A}$ increments. Assume $\beta_{\mathrm{DC}}=100$ and that $\mathrm{V}_{\mathrm{CE}}$ does not exceed breakdown.


Figure 4.15 For Example 5 [5]

## Solution:

Using the relationship $\mathrm{I}_{\mathrm{C}}=\beta_{\mathrm{DC}} \mathrm{I}_{\mathrm{B}}=100 \mathrm{I}_{\mathrm{B}}$, values of $\mathrm{I}_{\mathrm{C}}$ are calculated and tabulated in Table 4.1. The resulting curves are plotted in Figure 4.16.

Table 4.1

| $I_{B}$ | $I_{C}$ |
| :---: | :---: |
| $5 \mu \mathrm{~A}$ | 0.5 mA |
| $10 \mu \mathrm{~A}$ | 1.0 mA |
| $15 \mu \mathrm{~A}$ | 1.5 mA |
| $20 \mu \mathrm{~A}$ | 2.0 mA |
| $25 \mu \mathrm{~A}$ | 2.5 mA |



Figure 4.16 For Example 5 [5]

### 4.4.5 Cutoff

When $I_{B}=0$, the transistor is in the cutoff region of its operation. This is shown in Figure 4.17 with the base lead open, resulting in a base current of zero. Under this condition, there is very small of collector leakage current, $\mathrm{I}_{\text {CEO }}$, due mainly to thermally produced carriers. Because, $\mathrm{I}_{\text {CEO }}$ is extremely small, it will usually be neglected in circuit analysis so that $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CC}}$. Moreover, in cutoff mode, both the base-emitter and the base-collector junction are reverse-biased.


Figure 4.17 Cutoff mode [5]

### 4.4.6 Saturation

When the base-emitter junction becomes forward-biased and the basecurrent is increased, the collector current also increases and $\mathrm{V}_{\mathrm{CE}}$ decreases as a result of more drop across the collector resistor $\left(V_{C E}=V_{C C}-I_{C} R_{C}\right)$. This is illustrated in Figure 4.18. When $\mathrm{V}_{\mathrm{CE}}$ reaches its saturation value, $\mathrm{V}_{\mathrm{CE}(\text { sat) }}$, the basecollector junction becomes forward-biased and $\mathrm{I}_{\mathrm{C}}$ can increase no further even with a continued increase in $\mathrm{I}_{\mathrm{B}}$. And $\mathrm{V}_{\mathrm{CE}(\text { sat })}$ is usually only $0.2-0.3 \mathrm{~V}$ for silicon transistors.


Figure 4.18 Saturation mode. [5]

### 4.4.7 DC Load Line

Cutoff and saturation mode can be illustrated in relation to the collector characteristics curves by the use of a load line. Figure 4.19 shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point. The bottom of the load line is at ideal cutoff where $\mathrm{I}_{\mathrm{C}}=0$ and $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CC}}$. The top of the load line is at saturation where $\mathrm{I}_{\mathrm{C}}=\mathrm{I}_{\mathrm{C}(\text { sat) }}$ and $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CE}(\text { sat) }}$. In between cutoff and saturation along the load line is the active region of the transistor's operation.


Figure 4.19 DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions. [5]

Example 6: Determine whether or not the transistor in Figure 4.20 is in saturation. Assume $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}=0.2 \mathrm{~V}$.


Figure 4.20 For Example 6. [5]

## Solution:

$$
\begin{aligned}
& \begin{array}{l}
I_{C(s a t)}=\frac{V_{C C}-V_{C E(\text { sat })}}{R_{C}} \\
\quad=\frac{(10-0.2) V}{1 K \Omega}=9.8 \mathrm{~mA} \\
I_{B}= \\
V_{B B}-V_{B E} \\
R_{B}
\end{array}=\frac{3-0.7 V}{10 K \Omega}=0.23 \mathrm{~mA} \\
& \text { As } \beta_{D C} I_{B}=50^{*} 0.23 \mathrm{~mA}=11.5 \mathrm{~mA} \\
& I_{C(s a t)}
\end{aligned}
$$

$\therefore$ This transistor is operated in saturation mode.

Example 7: Determine whether or not the transistor in Figure 4.21 is in saturation. Assume $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}=0.2 \mathrm{~V}$.


Figure 4.21 For Example 7.

## Solution:

$$
\begin{aligned}
& V_{C C}=I_{C} R_{C}+V_{C E}+I_{E} R_{E}=I_{C} R_{C}+V_{C E}+\frac{I_{C}}{\alpha_{D C}} R_{E} \\
& \alpha_{D C}=\frac{\beta_{D C}}{\beta_{D C}+1}=\frac{50}{51}=0.98 \\
& V_{C C}=I_{C} R_{C}+V_{C E}+\frac{I_{C}}{0.98} R_{E}=I_{C} R_{C}+V_{C E}+1.02 I_{C} R_{E} \\
& I_{C}=\frac{V_{C C}-V_{C E}}{\left(R_{C}+1.02 R_{E}\right)} \\
& I_{C(s a t)}=\frac{V_{C C}-V_{C E(s a t)}}{R_{C}+1.02 R_{E}}=\frac{10-0.2 V}{1+1.02} 4.8 \mathrm{~mA} \\
& V_{B B}=I_{B} R_{B}+V_{B E}+I_{E} R_{E}=I_{B} R_{B}+0.7+\left(I_{B}+50 I_{B}\right) R_{E} \\
& I_{B}=\frac{V_{B B}-0.7}{R_{B}+51 R_{E}}=\frac{3-0.7 V}{(10+51 * 1) K \Omega}=0.038 \mathrm{~mA} \\
& I_{C}=\beta_{D C} I_{B}=50 * 0.038 \mathrm{~mA}=1.9 \mathrm{~mA}
\end{aligned}
$$

As $I_{C}<I_{C(s a t)} \quad \therefore$ This transistor is operated in active mode.

Example 8: Find Q-point when $\mathrm{V}_{\mathrm{BB}}=1 \mathrm{~V}, 2 \mathrm{~V}$ and 3 V . And then construct DC load line for this transistor. Assume $\mathrm{V}_{\mathrm{CE}(\text { sat })}=0 \mathrm{~V}$.


Figure 4.22 For Example 8. [5]

## Solution:

$$
\begin{aligned}
& I_{B}=\frac{V_{B B}-V_{B E}}{R_{B}}, I_{C}=\beta_{D C} I_{B}, V_{C E}=V_{C C}-I_{C} R_{C} \\
& \text { if } V_{B B}=1 ; I_{B}=\frac{1-0.7}{20 \mathrm{~K} \Omega}=0.015 \mathrm{~mA} \\
& \therefore I_{C}=50^{*} 0.015 \mathrm{~mA}=0.75 \mathrm{~mA} \\
& V_{C E}=10-(0.75 \mathrm{~mA})(1 \mathrm{~K} \Omega)=9.25 \mathrm{~V} \\
& \therefore Q_{1} i s a t V_{C E}=9.25 \mathrm{~V}, I_{C}=0.75 \mathrm{~mA} \\
& \text { if } V_{B B}=2 V ; I_{B}=\frac{2-0.7}{20 \mathrm{~K} \Omega}=0.065 \mathrm{~mA} \\
& \therefore I_{C}=50^{*} 0.065 \mathrm{~mA}=3.25 \mathrm{~mA} \\
& V_{C E}=10-(3.25 \mathrm{~mA})(1 \mathrm{~K} \Omega)=6.75 \mathrm{~V} \\
& \therefore Q_{2} \text { is at } V_{C E}=6.75 \mathrm{~V}, I_{C}=3.25 \mathrm{~mA} \\
& \text { if } V_{B B}=3 \mathrm{~V} ; I_{B}=\frac{3-0.7}{20 \mathrm{~K} \Omega}=0.115 \mathrm{~mA} \\
& \therefore I_{C}=50^{*} 0.115 \mathrm{~mA}=5.75 \mathrm{~mA} \\
& V_{C E}=10-(5.75 \mathrm{~mA})(1 \mathrm{~K} \Omega)=4.25 \mathrm{~V} \\
& \therefore Q_{3} \text { is at } V_{C E}=4.25 \mathrm{~V}, I_{C}=5.75 \mathrm{~mA}
\end{aligned}
$$

For cut off mode; $V_{C E}=V_{C C}=10 \mathrm{~V}\left(I_{C}=0\right)$
For saturation mode ;

$$
\begin{aligned}
& I_{C(s a t)}=\frac{V_{C C}-V_{C E(s a t)}}{R_{C}} \\
& \therefore I_{C(s a t)}=\frac{10-0}{1 K \Omega}=10 \mathrm{~mA}
\end{aligned}
$$



Figure 4.23 DC load line for Figure 4.22.

### 4.5 The Transistor as a Switch [5]

The basic operation as a switching device is illustrated in Figure 4.24. In part (a), the transistor is in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent. In part (b), the transistor is in the saturation region because the base-emitter junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector to reach its saturation value.

In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent. Actually, a voltage drop of up to a few tenths of a volt normally occurs, which is the saturation voltage, $\mathrm{V}_{\mathrm{CE}(\text { sat })}$.

## Conditions in Cutoff:

As mentioned before, a transistor is in the cutoff region when the baseemitter junction it not forward-biased. Neglecting leakage current, all of the currents are zero, and $\mathrm{V}_{\mathrm{CE}}$ is equal to $\mathrm{V}_{\mathrm{CC}}$. Or $\mathrm{V}_{\mathrm{CE} \text { (cutoff) }}=\mathrm{V}_{\mathrm{CC}}$

## Conditions in Saturation:

When the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is

$$
I_{C(s a t)}=\frac{V_{C C}-V_{C E(s a t)}}{R_{C}}
$$

$$
\text { since } V_{C E(s a t)} \text { is verysmall and can usuallybe neglected }
$$

The minimum value of base current needed to produce saturation is

$$
I_{B(\min )}=\frac{I_{C(\mathrm{sat})}}{\beta_{D C}}
$$

$\mathrm{I}_{\mathrm{B}}$ should be significantly greater than $\mathrm{I}_{\mathrm{B}(\min )}$ to keep the transistor well into saturation.

(a) Cutoff - open switch

(b) Saturation - closed switch

Figure 4.24 Switching action of an ideal transistor. [5]

## Example 9:

(a) For the transistor circuit in Figure 4.25 , what is $\mathrm{V}_{\mathrm{CE}}$ when $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ ?
(b) What minimum value of $I_{B}$ is required to saturate this transistor if $\beta_{D C}$ is 200 ? Neglect $\mathrm{V}_{\mathrm{CE}(\text { sat })}$.
(c) Calculate the maximum value of $\mathrm{R}_{\mathrm{B}}$ when $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$.


Figure 4.25 For Example 9. [5]

## Solution:

(a) When $V_{I N}=0 V$, the transistor is in cutoff (acts like an open switch) and $V_{C E}=V_{C C}=10 \mathrm{~V}=V_{C E(\text { cutoff })}$
(b) Since $V_{C E(s a t)}$ is neglected
$I_{C(\text { sat })}=\frac{V_{C C}}{R_{C}}=\frac{10 \mathrm{~V}}{1.0 \mathrm{~K} \Omega}=10 \mathrm{~mA}$
$I_{B(\text { min })}=\frac{I_{C(\text { sat })}}{\beta_{D C}}=\frac{10 \mathrm{~mA}}{200}=50 \mu \mathrm{~A}$
(c) When the transistor is on. $V_{B E} \cong 0.7 V$ and
$V_{R_{B}}=V_{I N}-V_{B E}=5-0.7 \mathrm{~V}=4.3 \mathrm{~V}$
Calculate the maximum value of $R_{B}$ needed to allow a minimum $I_{B}$ of $50 \mu \mathrm{~A}$ by Ohm's law as follow

$$
R_{B(\max )}=\frac{V_{R B}}{I_{B(\min )}}=\frac{4.3}{50 \mu \mathrm{~A}}=86 \mathrm{~K} \Omega
$$

## A Simple Application of a Transistor Switch:

The transistor shown in Figure 4.26 is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated. When the square wave is at 0 V , the transistor is in cutoff and, since there is no collector current, the LED does not emit light. When the square wave goes to its high level, the transistor saturates. This forward-bases the LED, and the resulting collector through the LED causes it to emit light. So, we have a blinking LED that is on for 1 s and off for 1 s .


Figure 4.26 A transistor used to switch an LED on and off. [5]

Example 10: The LED in Figure 4.27 requires 30 mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30 mA . For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of base current as a safety margin to ensure saturation. $\mathrm{V}_{\mathrm{CC}}=9 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}(\mathrm{sat})}=0.3 \mathrm{~V}$, $\mathrm{RC}=270 \Omega, \mathrm{RB}=3.3 \mathrm{k} \Omega$, and $\beta_{\mathrm{DC}}=50$.


Figure 4.27 For Example 10. [5]

## Solution:

$$
\begin{aligned}
& I_{C(\text { sat })}=\frac{V_{C C}-V_{C E(\text { sat })}}{R_{C}}=\frac{9 \mathrm{~V}-0.3 \mathrm{~V}}{270 \Omega}=32.2 \mathrm{~mA} \\
& I_{B(\min )}=\frac{I_{C(\text { sat })}}{\beta_{D C}}=\frac{32.2 \mathrm{~mA}}{50}=644 \mu \mathrm{~A}
\end{aligned}
$$

To ensure saturation, use twice the value of $I_{B(\min )}$, which gives 1.29 mA .
Then; $\quad I_{B}=\frac{V_{R_{B}}}{R_{B}}=\frac{V_{I N}-V_{B E}}{R_{B}}=\frac{V_{I N}-0.7}{3.3 K \Omega}$
$V_{I N}-0.7 V=2 I_{B(\min )} R_{B}$
$V_{I N}=(1.29 \mathrm{~mA})(3.3 \mathrm{~K} \Omega)+0.7 \mathrm{~V}=4.96 \mathrm{~V}$
\#

### 4.6 Homework 7

1. Determine each current in this figure. What is the $\beta_{\mathrm{DC}}$ ?


Figure 4.28 For problem 1. [5]
2. Find $V_{C E}, V_{B E}$, and $V_{C B}$ in both circuits.


Figure 4.29 For problem 2. [5]
3. Find $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{E}}$ and $\mathrm{I}_{\mathrm{C}}$. Assume $\alpha_{\mathrm{DC}}=0.98$.


Figure 4.30 For problem 3. [5]
4. Find $\mathrm{R}_{\mathrm{B}}$ in this circuit that make the transistor to operate under the linear mode or the saturation mode. Assume $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}=0.2 \mathrm{~V}$ and $\beta_{\mathrm{DC}}=100$.


Figure 4.31 For problem 4.
5. (a) The LED in this circuit requires 25 mA to emit a sufficient amount of light. Therefore, the collector current ( $\mathrm{I}_{\mathrm{C}}$ ) should be greater than or equal to 25 mA . For the following circuit values, determine the amplitude of the square wave input voltage ( $\mathrm{V}_{\mathrm{IN}(\text { max })}$ ) necessary to make sure that the transistor saturates. Use $\mathrm{I}_{\mathrm{B}}=2 \times \mathrm{I}_{\mathrm{B}(\min )}$ as a safety margin to ensure saturation. Here, $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$, $\mathrm{V}_{\mathrm{CE}(\text { sat })}=0.2 \mathrm{~V}, \mathrm{R}_{\mathrm{C}}=500 \Omega, \mathrm{R}_{\mathrm{B}}=5 \mathrm{k} \Omega$ and $\beta_{\mathrm{DC}}=100$.
(b) Suppose that you change the LED to one that requires 40 mA for a specified light emission and that you are not allowed to modify any component in the transistor switch circuit. In this case, can you use this transistor as a switch to turn on and off the LED?
(c) Suppose that you still use the LED that requires 40 mA for a specified light emission from (b), but that you are not allowed to increase the input amplitude above $\mathrm{V}_{\mathrm{IN}(\max )}$ that you calculated from (a) and $\mathrm{V}_{\mathrm{CC}}$ above 15 V . However, you are allowed to modify the circuit by changing $\mathrm{R}_{\mathrm{B}}$ and $\mathrm{R}_{\mathrm{C}}$. Then, how would you modify the circuit to use the transistor as the switch to turn on and off the LED? Specify each component to be changed and its corresponding value. Here, assume $\mathrm{I}_{\mathrm{B}}=2 \times \mathrm{I}_{\mathrm{B}(\min )}$ as a safety margin to ensure saturation.


Figure 4.32 For problem 5. [5]
6. If $\beta_{\mathrm{DC}}=100$, find $\mathrm{V}_{\mathrm{OUT}}, \mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}$ and $\mathrm{I}_{\mathrm{RL}}$ for
(a) $V_{B B}=0 \mathrm{~V}$
(b) $\mathrm{V}_{\mathrm{BB}}=1 \mathrm{~V}$


Figure 4.33 For problem 6.
7. For the transistor in this figure, $\beta_{D C}=30$. Determine $V_{1}$ such that $V_{C E}=6 \mathrm{~V}$.


Figure 4.34 For problem 7.
8. Consider the circuit shown in Figure 4.35. Assume $\beta_{\mathrm{DC}}=50, \mathrm{~V}_{\mathrm{CE}(\text { sat })}=0 \mathrm{~V}$ and $\mathrm{I}_{\mathrm{C}(\mathrm{cut} \mathrm{off)}}=0 \mathrm{~A}$.
(a) Let $\mathrm{V}_{\mathrm{BB}}=15 \mathrm{~V}$, determine the Q-point value of $\mathrm{I}_{\mathrm{C}}$ and $\mathrm{V}_{\mathrm{CE}}$ in the circuit.
(b) Determine the value of $\mathrm{V}_{\mathrm{BB}}$ to make $\mathrm{I}_{\mathrm{C}} / \mathrm{I}_{\mathrm{B}}=10$, then calculate $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}$ and $\mathrm{I}_{\mathrm{E}}$.


Figure 4.35 For problem 8.
9. Consider the circuit shown in Figure 4.36. Assume $\beta_{D C}=100$,
(a) Let $\mathrm{V}_{\mathrm{BB}}=5 \mathrm{~V}$, determine $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}, \mathrm{I}_{\mathrm{E}}, \mathrm{I}_{\mathrm{RL}}$ and $\mathrm{V}_{\mathrm{CE}}$ in the circuit.
(b) What minimum value of $\mathrm{V}_{\mathrm{BB}}$ is required to saturate this transistor? Assume $\mathrm{V}_{\mathrm{CE}(\text { sat })}=0 \mathrm{~V}$ and $\mathrm{I}_{\mathrm{C}} \cong \mathrm{I}_{\mathrm{E}}$.


Figure 4.36
10. For the transistor in Figure 4.37, $\beta_{\mathrm{DC}}=50$. Determine $\mathrm{V}_{1}$ such that $\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}$. Then calculate $\mathrm{V}_{\mathrm{EC}}$ in the circuit. Using $\mathrm{I}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}}+\mathrm{I}_{\mathrm{C}}$.


Figure 4.37

